

1. Title: Simulation of Second Order Effect Signatures of Integrated Circuits

2. Individual Sponsor:

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3. Academic Area/Field and Education Level: physics, electrical engineering (MS or PhD)

4. Objective: Develop methodologies and models to simulate the expected second order effect (2OE) signature from the design files of an integrated circuit to replace the need for a golden reference device in 2OE assurance testing.

5. Description: Second order effect (2OE) measurement systems have shown sensitivity to minor differences within Integrated Circuits (IC) thus demonstrating potential utility for detecting counterfeit microelectronics devices. Such methodologies are based on differentiating device physical behaviors and require a known good “golden” sample device as a reference. However, relying on golden sample devices carries certain assurance risks based on assumptions about the golden devices. This topic aims to investigate whether 2OE signals and signatures can be predicted and modeled from first principles physics simulations based on design files (GDSII, SPICE models, netlist, etc.) of a device under test (DUT). Successful simulation of the 2OE may alleviate the current requirement of a golden device for comparison with 2OE measurements. Additionally, these 2OE models will be useful to validate digital twin models of target devices and systems, and advance design of secure systems.

6: Research Classification/Restriction: CUI/ITAR

7. Eligible Research Institutions: All

Keywords: Second Order Effects, Side Channel Analysis, Digital Twin, Modeling, Simulation, Digital Engineering, Integrated Circuits